N-13

DESIGN AND PERFORMANCE OF DUAL-GATE GaAs MESFET UP-CONVERTER

A.A. de Salles
CETUC-Universidade Católica
Rua Marques de São Vicente 209
Rio de Janeiro 22453 RJ-BRASIL

ABSTRACT

Design procedure and experimental results for a GaAs MESFET Up-Converter using a dual gate device are presented. DC and S parameter measurements are used to estimate the appropriate biasing and matching conditions. High conversion gain (~8dB) and moderate noise performance (~7dB) were obtained.

INTRODUCTION

Operation of dual-gate GaAs MESFET as down converters has already been demonstrated [1],[2]. Although these mixers present adequate conversion gain and simplicity in the mixer circuitry, the noise performance has been a main drawback. However, the noise requirements for up-converters (transmitters) are generally less restricted in comparison to those for down converters (receivers) encouraging therefore the development of dual-gate FET up-converters [3]. Also, the higher frequencies involved (in the GHz range) imply a negligible contribution of the 1/f noise and trapping, which has been recognized to be of importance in low IF frequency down-converters [1], [4] and [5].

Simple design procedure based on the DC characteristics and on the directly measurable S parameters is presented in the first part of the work.

The second part deals with the experimental results. To this an up-converter using a NEC dual-gate GaAs MESFET type NE46385 was designed to operate at an input signal frequency of 1,042.5 MHz, a local oscillator frequency of 5 GHz and an output signal of 6,042.5 GHz. Input/output microstrip lines on Rogers type 6010 substrate (ε_r = 10.5 and H = 0.635mm) were employed.

DESIGN PROCEDURE

Fig. 1 illustrates a schematical cross section of the intrinsic dual-gate FET and the correspondent circuit elements [6].

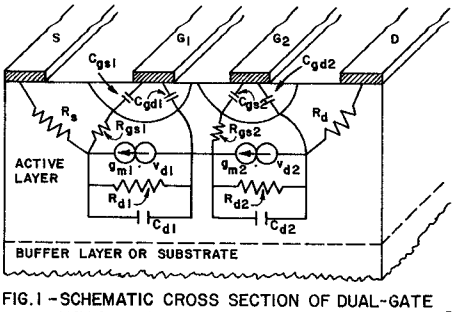

FIG.1 - SCHEMATIC CROSS SECTION OF DUAL-GATE MESFET WITH INTRINSIC CIRCUIT ELEMENTS [6].

Figs. 2(a) and (b) show the characteristics of the dual-gate device for different voltages at gates 1 and 2 respectively.

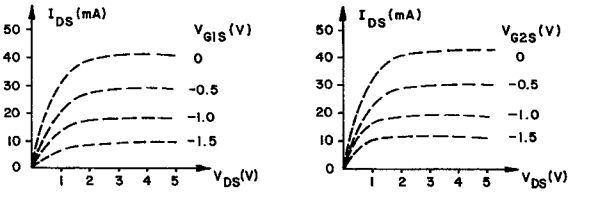

FIG.2 - DUAL-GATE MESFET DC CHARACTERISTICS - (a) V_{G2S} = OV; (b) V_{G1S} = OV.

Fig. 3 illustrates the variation of the transfer characteristics of the dual-gate device in function of gate 1 and gate 2 bias voltages, at V_{DS} = 4 volts.

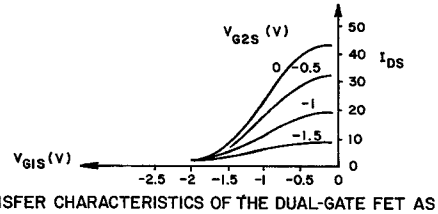

FIG.3 - TRANSFER CHARACTERISTICS OF THE DUAL-GATE FET AS A FUNCTION OF THE BIAS OF BOTH GATES, AT A DRAIN VOLTAGE OF 5V.

From these curves the transconductance characteristics g_{m1} versus V_{G1S} and g_{m2} versus V_{G2S} were calculated and are shown in Figs. 4 and 5, respectively.

Modulation of both g_{m1} and g_{m2} by variations of gate 1 and gate 2 voltages are clearly confirmed in these graphs. The best bias point for gate 1 is predicted to be where a maximum g_{m1} variation can be achieved within extreme limits of V_{G2S} values (V_{G1S} ~ 1V).

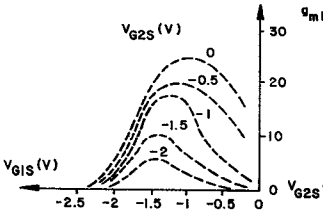

FIG.4 - g_{m1} x V_{G1S} CHARACTERISTICS

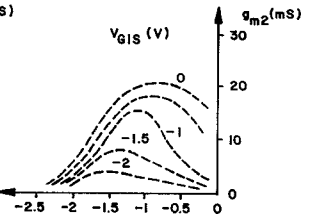

FIG.5 - g_{m2} x V_{G2S} CHARACTERISTICS

When the input signal at f_{sig} is fed into gate 1 and the local oscillator signal at f_{LO}

0149-645X/83/0000-0187 $01.00 © 1983 IEEE

is fed into gate 2, the output signal at the drain contains the mixing products of these two frequencies. Dual-gate FET up converter circuit is shown in Fig.6. An interdigital band-pass filter at the output port selects the summing frequency ($f_{LO} + f_{sig}$) and can also be used as an impedance transformer and DC break.

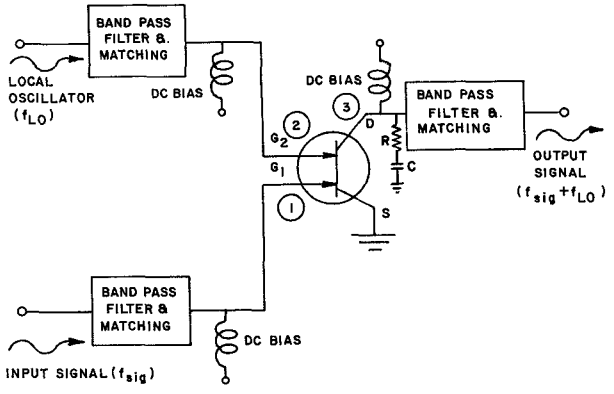

FIG.6 - DUAL-GATE FET UP CONVERTER SCHEMATIC CIRCUIT

Matching of input and output ports at the desired frequencies is easily accomplished from the measured S parameters. Tables 1 and 2 illustrate the measured small signal S parameters of the NEC dual-gate GaAs MESFET NE 46385 (common source) from 1 to 8 GHz, for gate bias V_{G1S} = 0V; V_{G2S}= 0V and V_{G1S}= -1V; V_{G2S}= -1V respectively, and drain bias V_{DS} of 4 volts. S parameters are referred to the FET terminals.

As the S parameters are related by analytical formulas to the Y parameters, approximate values for some circuit parameters (Fig. 1) at that bias point can be obtained. Therefore, the conversion gain can be estimated from [7],

$$G_C = \frac{g_{m1}^2}{4\omega^2 \bar{C}_{gS1}^2} \quad \frac{\bar{R}_d}{R_{in}} \qquad (1)$$

where $\bar{C}_{gS1}$ and $\bar{R}_d$ represent the time averaged values of the source-to-gate 1 capacitance and drain resistance respectively.

PERFORMANCE

The occurence of instabilities (oscillations) and spurius were investigated. A damping chip resistor is added to the output circuit(Fig.6) to ensure unconditional stability (K>1). This however reduces the conversion gain. Also, the interdigital filter introduces an insertion loss of around 1dB in the pass band, degrading therefore the gain and noise performance by the same amount.

Experimental results under optimized matching conditions, measured at a signal frequency of 1,042.5 MHz, local oscillator frequency of 5GHz and output frequency of 6,042.5 MHz are shown in Figs. 7 to 11.

The conversion gain is strongly dependent upon the bias condictions. Figs. 7 and 8 illustrate the conversion gain versus gate 1 and gate 2 voltages respectively.

MEASURED SMALL SIGNAL S PARAMETERS OF THE DUAL GATE FET

FREQ. (GHz)	S_{11}		S_{13}		S_{31}		S_{33}	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
TABLE 1: V_{DS} = 4V; V_{G1S} = 0V; V_{G2S} = 0V								
1	0.95	-34	0.02	61	1.80	155	0.84	-21
2	0.94	-50	0.03	46	1.65	131	0.83	-35
3	0.91	-72	0.04	33	1.66	97	0.83	-47
4	0.87	-89	0.05	25	1.71	78	0.74	-61
5	0.84	-115	0.05	5	1.62	51	0.77	-89
6	0.85	-148	0.06	-2	1.86	37	0.78	-98
7	0.81	165	0.06	-30	1.61	1	0.78	-132
8	0.75	+163	0.05	-49	1.36	-27	0.76	-147
TABLE 2: V_{DS} = 4V; V_{G1S} = -1V; V_{G2S} = -1V								
1	0.98	-30	0.02	60	1.60	142	0.90	-20
2	0.96	-45	0.03	45	1.50	119	0.88	-33
3	0.94	-65	0.04	32	1.57	91	0.88	-44
4	0.90	-82	0.05	24	1.60	71	0.80	-57
5	0.88	-108	0.055	5	1.50	43	0.84	-84
6	0.87	-140	0.065	-2	1.73	30	0.84	-90
7	0.83	-157	0.065	-32	1.54	-6	0.84	-123
8	0.78	+170	0.05	-50	1.28	-31	0.82	-137

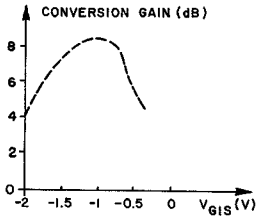

FIG.7- CONVERSION GAIN VERSUS GATE 1 BIAS (V_{DS}=4V; V_{G2S}=-1.2V; f_{LO}=5 GHz; f_{sig}=1GHz; LO LEVEL 10dBm INPUT LEVEL=-18dBm)

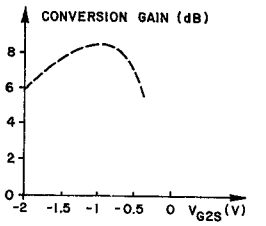

FIG.8-CONVERSION GAIN VERSUS GATE 2 (V_{DS}=4V; V_{G1S}=-1.2V; f_{LO}= 5GHz, f_{sig}=1GHz; LO LEVEL = 10 dBm; INPUT LEVEL=-18dBm)

Optimum bias voltage of $V_{G1S} \cong -1.2V$ and $V_{G2S} \cong -1.2V$ are close to the predicted values. The subsequent measurements were performed under these optimum bias conditions.

Fig. 9 shows the variation of conversion gain with local oscillator drive.

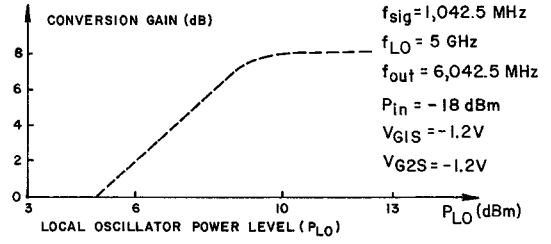

FIG. 9-Up CONVERTER CONVERSION GAIN VERSUS LO POWER LEVEL.

There is a limiting value (~8dBm)over which no improvement in gain can be obtained.

Fig. 10 illustrates the conversion gain versus signal input level.

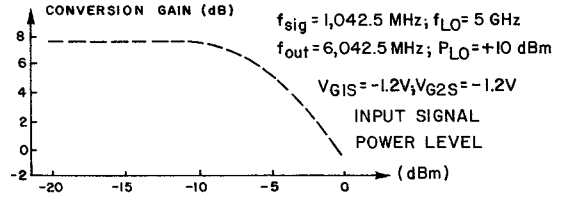

FIG. 10 - Up CONVERTER CONVERSION GAIN VERSUS SIGNAL INPUT POWER.

The 1dB compression point is around -6dBm. Output power at 1dB compression point is around + 1dBm.

Fig. 11 shows the dependence of the measured SSB noise figure with local oscillator power. An AILTECH (type 75) Precision Automatic Noise Figure Indicator was used.

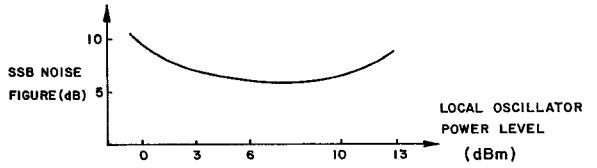

FIG.11- MEASURED SSB NOISE FIGURE F_{SSB} VERSUS LOCAL OSCILLATOR POWER P_{LO} (PARAMETERS AS IN FIG. 9).

The noise figure presents a broad flat minumum of around 7dB. This uses the same bias conditions as those for the conversion gain measurements (Fig.9). It was observed that the optimum gate bias conditions for best noise figure differ from the optimum bias conditions for maximum conversion gain. This is not yet fully understood.

CONCLUSIONS

The dual-gate GaAs MESFET Up-Converter has the following convenient features:

- moderate noise figure
- high conversion gain
- relative simplicity in the mixer circuit

A simple design procedure based on DC and S parameters measurements is described from which proper matching and optimum bias point are easily obtained.

Experimental results have shown a conversion gain of around 8dB and a noise figure of around 7dB.

This device may find applications in monolithic microwave integrated circuits.

ACKNOWLEDGEMENTS

This work received financial support from TELEBRAS (Telecomunicações Brasileiras S/A) under contract nº 88/82. The author is gratefull to Miss D.Consoni and Dr.J.K.C.Pinto (both from Univ. of. São Paulo) for useful suggestions and for lending some extra FET samples. Mr.L.F.M.Conrado and Mr. M.M. Mosso's assistance during the experiments is also gratefully acknowledged.

REFERENCES:

[1] S.C.Cripps et al., "An Experimental Evaluation of X-band Mixers using Dual-gate GaAs MESFET", - Proc. 7th.Europ.Micr. Conference, Copenhagen, 1977, pp.101-104.

[2] C. Tsironis et al., "A Self-oscillating Dual-gate MESFET X-band Mixer with 12dB Conversion-gain", Proc. 9th. Europ. Micr. Conf., 1979, Brighton, England, pp.321-325.

[3] W.C. Tsai et al., "Switching & Frequency Conversion Using Dual-Gate FETs", Proc. 9th. Europ. Micr. Conf., 1979, Brighton, England, pp. 311-315.

[4] B. Loriou and J.C.Leost, "Design and Performance of Low Noise C and X-band GaAs FET Mixers",Proc. 7th. Europ. Micr. Conf., Copenhagen, 1977, pp. 95-100.

[5] D. Consoni, "Microwave Integrated Circuit Image Rejection Mixer", M.Sc. thesis, University College London, 1980.

[6] C. Tsironis and R. Meierer, "Microwave Wide-Band Model of GaAs Dual Gate MESFET's", IEEE Transactions on MTT, vol. MTT-30, nº 3, March 1982, pp. 243-251.

[7] R.Pucel et al., "Performance of GaAs MESFET Mixers at X-band", IEEE Transactions on MTT, vol. MTT-24, nº 6, June 1976, pp.351--360.